CQNE36132

25V Dual Asymmetric N-Channel MOSFET

General Description

- Bottom Source Technology
- Very Low $R_{DS(ON)}$
- High Current Capability
- RoHS and Halogen-Free Compliant

Applications

- DC/DC Converters in PC, Servers
- Point of load Converters

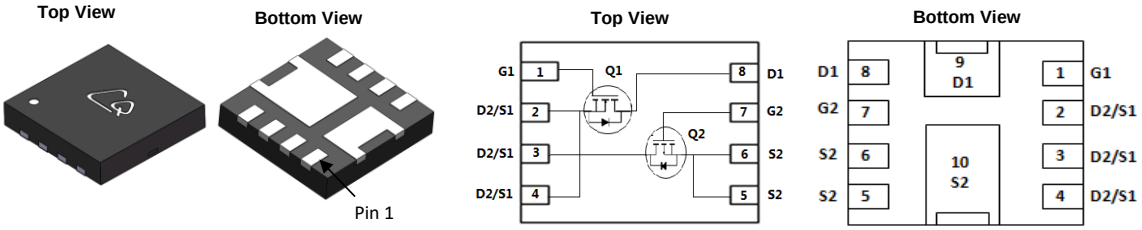
Product Summary

	Q1	Q2
V_{DS}	25V	25V
I_D (at V_{GS}=10V)	17A	34A
$R_{DS(ON)}$ (at V_{GS}=10V)	< 4.6mΩ	< 1.4mΩ
$R_{DS(ON)}$ (at V_{GS}=4.5V)	< 6mΩ	< 1.7mΩ

100% UIS Tested
100% Rg Tested

Green Product

DFN3.3x3.3A



Orderable Part Number	Package Type	Form	Minimum Order Quantity
CQNE36132	DFN3.3x3.3A	Tape & Reel	3000

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Max Q1	Max Q2	Units
Drain-Source Voltage		V_{DS}	25	25	V
Gate-Source Voltage		V_{GS}	±12	±12	V
Continuous Drain Current	T_C=25°C	I_D	60[G]	60[G]	A
	T_C=100°C		38	60[G]	
Pulsed Drain Current [C]		I_{DM}	160	200	
Continuous Drain Current	T_A=25°C	I_{DSM}	17	34	A
	T_A=70°C		13.5	27	
Avalanche Current [C]		I_{AS}	48	60	A
Avalanche energy	L=0.01mH [C]	E_{AS}	12	18	mJ
Power Dissipation [B]	T_C=25°C	P_D	25	35.5	W
	T_C=100°C		10	14	
Power Dissipation [A]	T_A=25°C	P_{DSM}	2	2.5	W
	T_A=70°C		1.3	1.6	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150		°C

Thermal Characteristics

Parameter		Symbol	Typ Q1	Typ Q2	Max Q1	Max Q2	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	50	40	60	50	°C/W
Maximum Junction-to-Ambient [A D]	Steady-State		75	65	90	80	°C/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	4	2.5	5	3.5	°C/W

Q1 Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V	25			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=25V, V_{GS}=0V			1	µA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±12V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=$V_{GS,}$ I_D=250µA	1	1.4	1.8	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=17A		3.8	4.6	mΩ
		T_J=125°C		5.3	6.4	
		V_{GS}=4.5V, I_D=15A		4.8	6	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=17A		100		S
V_{SD}	Diode Forward Voltage	I_S=1A, V_{GS}=0V		0.7	1	V
I_S	Maximum Body-Diode Continuous Current				30	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=12.5V, f=1MHz		880		pF
C_{oss}	Output Capacitance			250		pF
C_{rss}	Reverse Transfer Capacitance			55		pF
R_g	Gate resistance	f=1MHz	0.35	0.7	1.05	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=12.5V, I_D=17A		14.5	21	nC
Q_g(4.5V)	Total Gate Charge			6.5	10	nC
Q_{gs}	Gate Source Charge			2.5		nC
Q_{gd}	Gate Drain Charge			2.5		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=12.5V, R_L=0.75Ω, R_{GEN}=3Ω		4.5		ns
t_r	Turn-On Rise Time			3.5		ns
$t_{D(off)}$	Turn-Off DelayTime			20		ns
t_f	Turn-Off Fall Time			2.5		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=17A, di/dt=500A/µs		9		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=17A, di/dt=500A/µs		11.5		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ t≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Single pulse width limited by junction temperature $T_{J(MAX)}$=150° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.
G. The maximum current rating is package limited.
H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

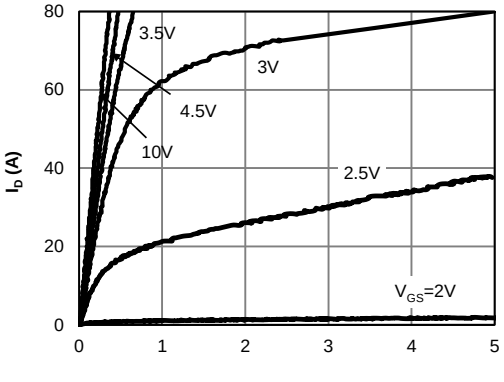


Figure 1: On-Region Characteristics (Note E)

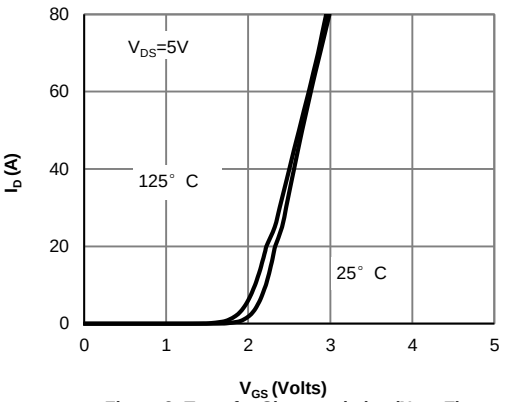


Figure 2: Transfer Characteristics (Note E)

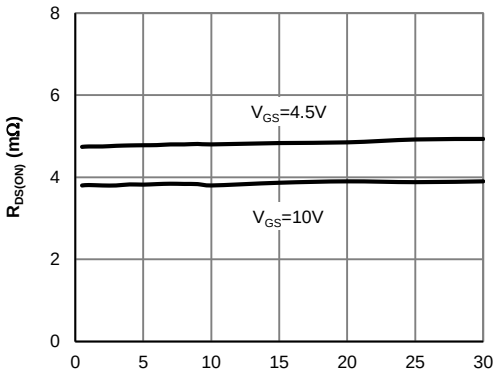


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

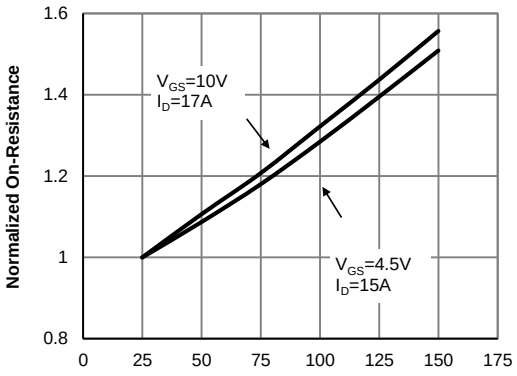


Figure 4: On-Resistance vs. Junction Temperature (Note E)

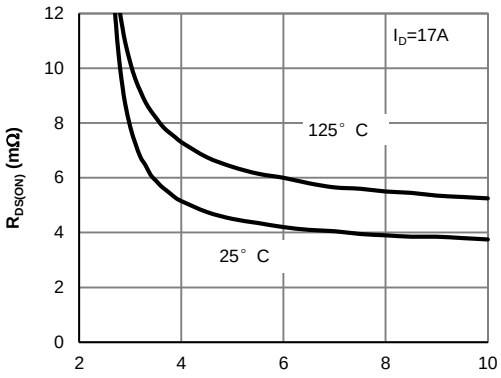


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

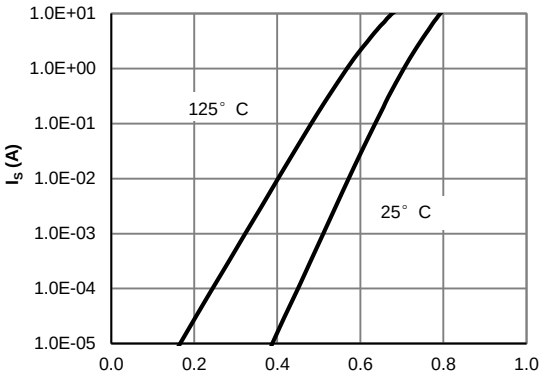


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

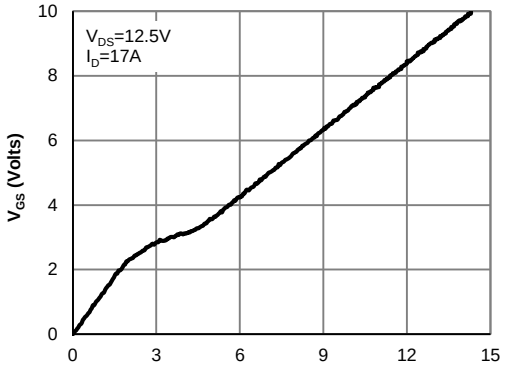


Figure 7: Gate-Charge Characteristics

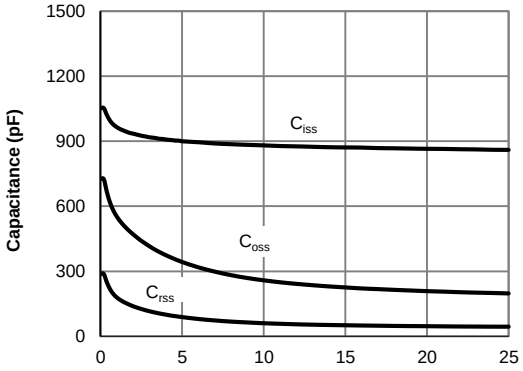
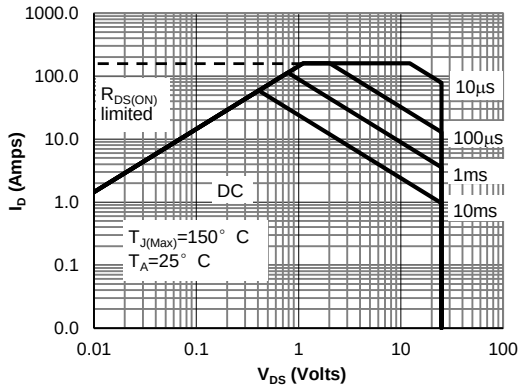


Figure 8: Capacitance Characteristics



V_{GS}> or equal to 4.5V

Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

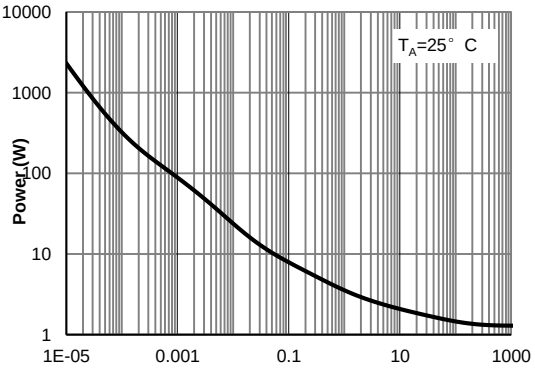


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note H)

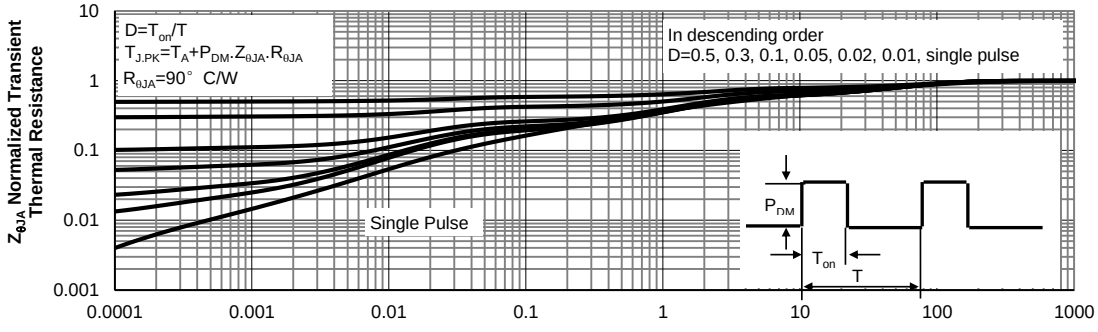


Figure 11: Normalized Maximum Transient Thermal Impedance (Note H)

Q2 Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V	25			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=25V, V_{GS}=0V			1	µA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±12V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=$V_{GS,}$ I_D=250µA	1	1.4	1.8	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=20A		1.1	1.4	mΩ
		T_J=125°C		1.5	1.9	
		V_{GS}=4.5V, I_D=20A		1.3	1.7	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=20A		165		S
V_{SD}	Diode Forward Voltage	I_S=1A, V_{GS}=0V		0.7	1	V
I_S	Maximum Body-Diode Continuous Current				40	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=12.5V, f=1MHz		3215		pF
C_{oss}	Output Capacitance			860		pF
C_{rss}	Reverse Transfer Capacitance			200		pF
R_g	Gate resistance	f=1MHz	0.4	0.8	1.2	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=12.5V, I_D=20A		55	80	nC
Q_g(4.5V)	Total Gate Charge			25	35	nC
Q_{gs}	Gate Source Charge			9.5		nC
Q_{gd}	Gate Drain Charge			5		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=12.5V, R_L=0.6Ω, R_{GEN}=3Ω		8		ns
t_r	Turn-On Rise Time			5.5		ns
$t_{D(off)}$	Turn-Off DelayTime			39.5		ns
t_f	Turn-Off Fall Time			7		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=20A, di/dt=500A/µs		16		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=20A, di/dt=500A/µs		33.5		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ t≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Single pulse width limited by junction temperature $T_{J(MAX)}$=150° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.
G. The maximum current rating is package limited.
H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

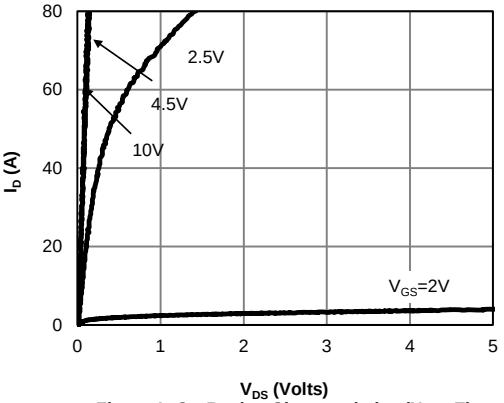


Figure 1: On-Region Characteristics (Note E)

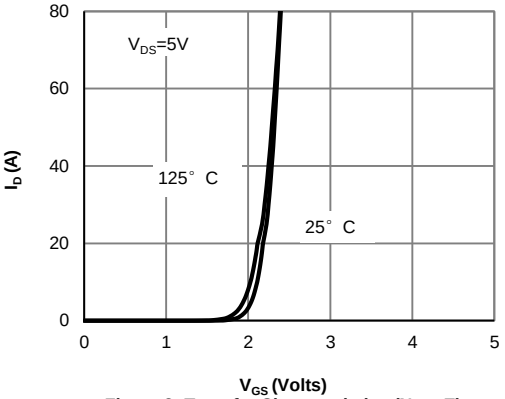


Figure 2: Transfer Characteristics (Note E)

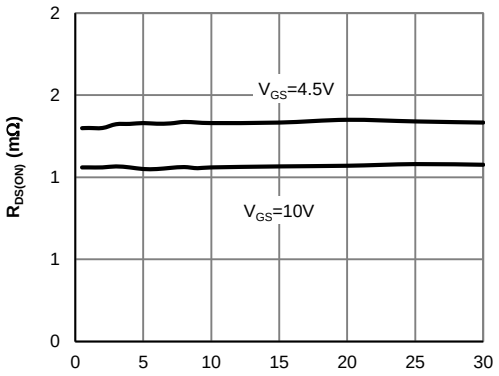


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

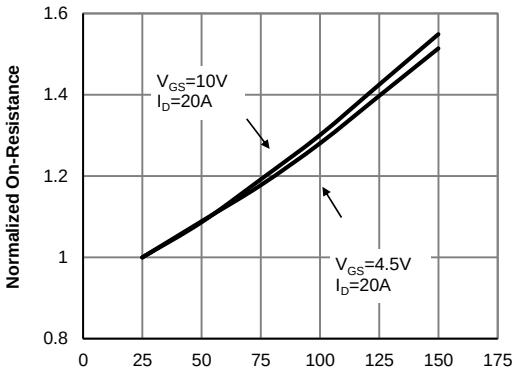


Figure 4: On-Resistance vs. Junction Temperature (Note E)

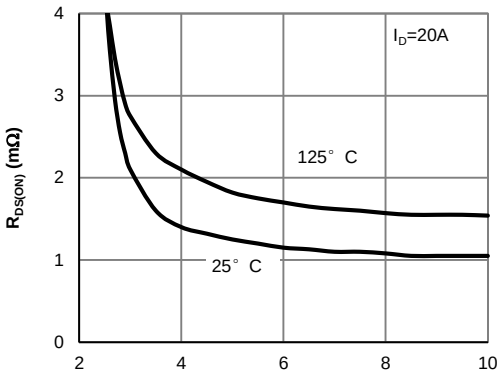


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

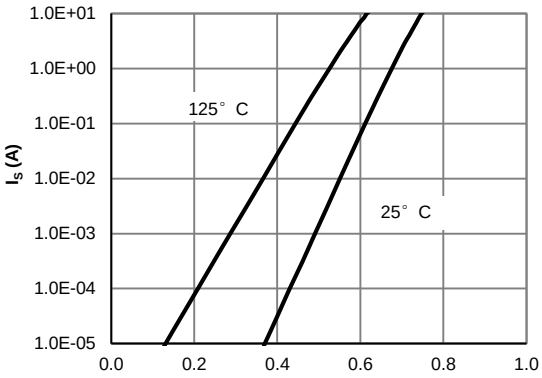


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

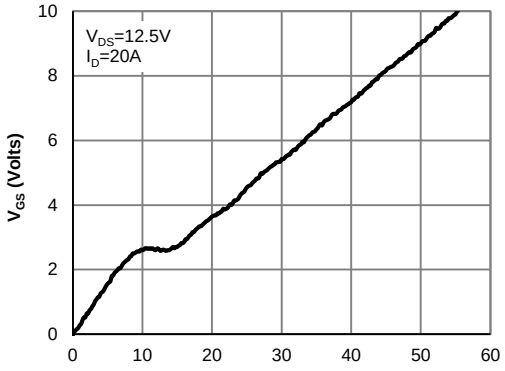


Figure 7: Gate-Charge Characteristics

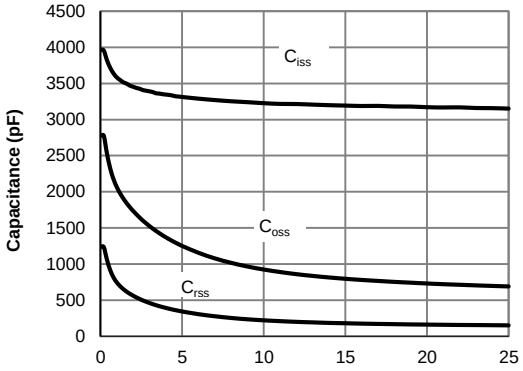


Figure 8: Capacitance Characteristics

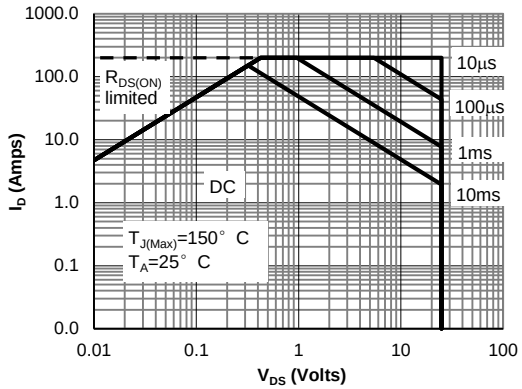


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

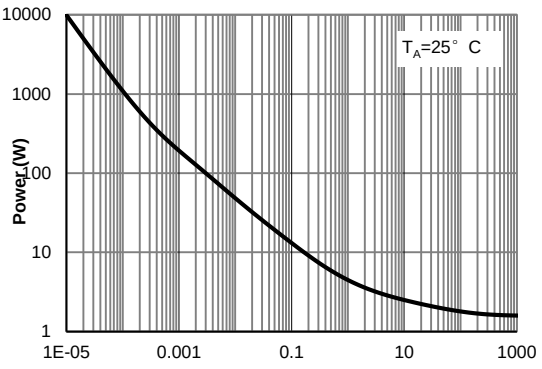


Figure 13: Single Pulse Power Rating Junction-to-Ambient (Note H)

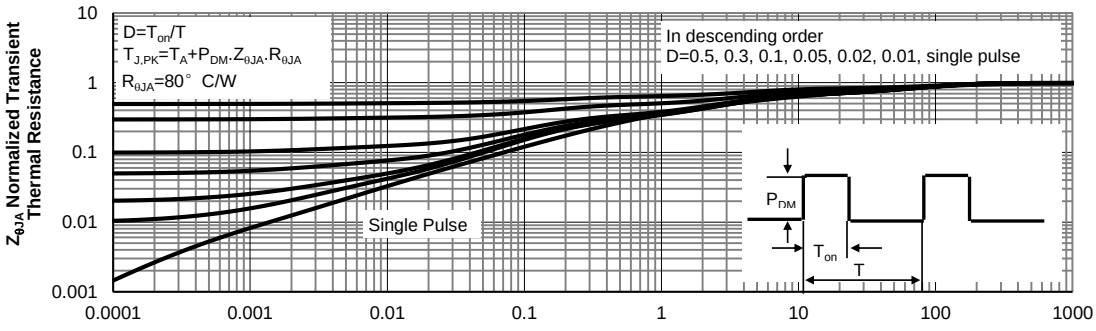


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

Figure A: Gate Charge Test Circuit & Waveforms

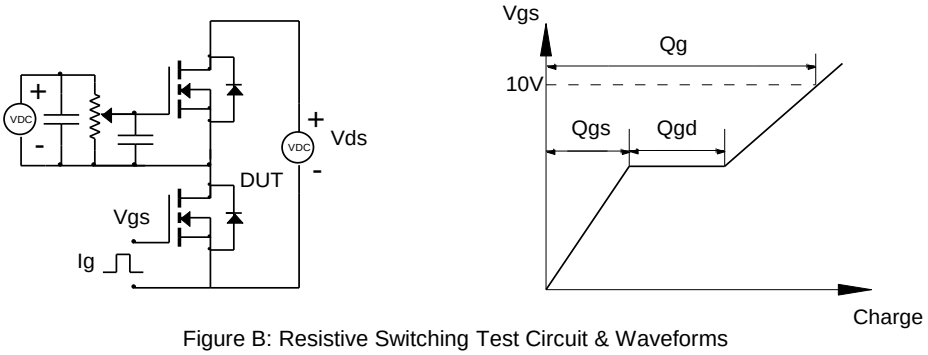


Figure B: Resistive Switching Test Circuit & Waveforms

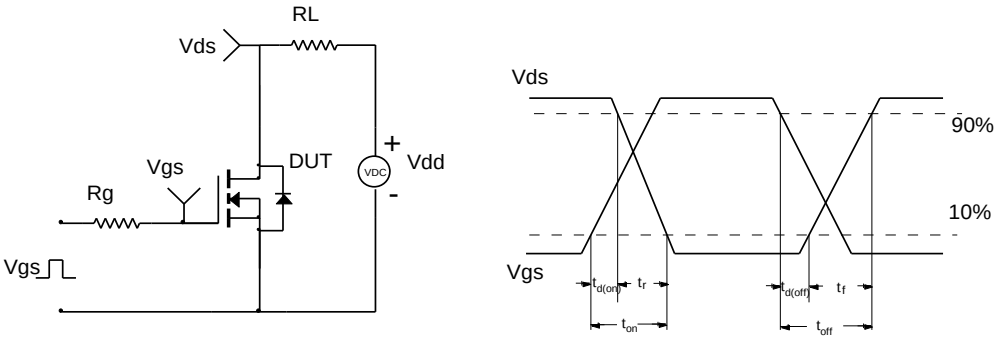


Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

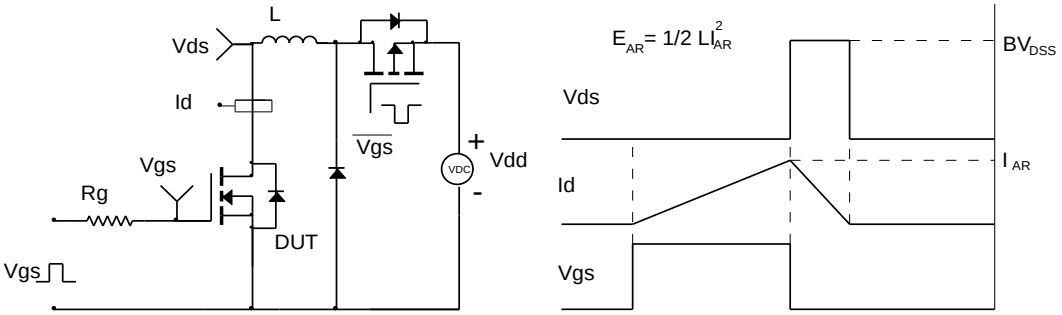
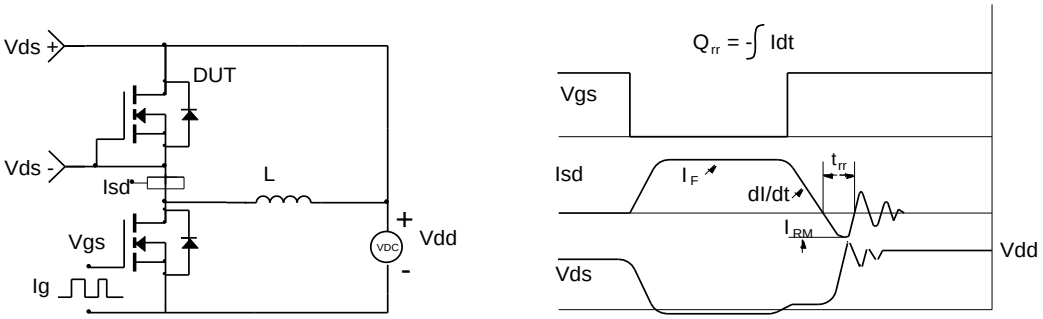


Figure D: Diode Recovery Test Circuit & Waveforms



Document No.	PDCQ-00019
Version	A
Title	CQNE36132 Marking Description

DFN3.3x3.3A PACKAGE MARKING DESCRIPTION

Green product

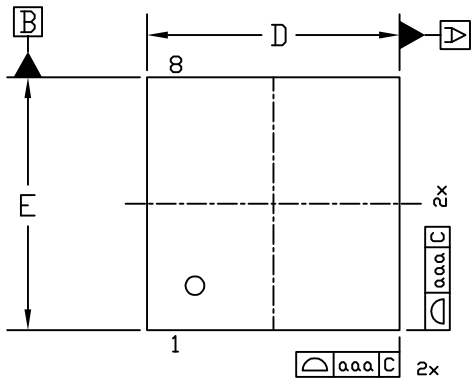
NOTE:
LOGO - CQAOS Logo
36132 - Part number code
F - Fab code
A - Assembly location code
Y - Year code
W - Week code
L&T - Assembly lot code

PART NO.	DESCRIPTION	CODE
CQNE36132	Green product	36132

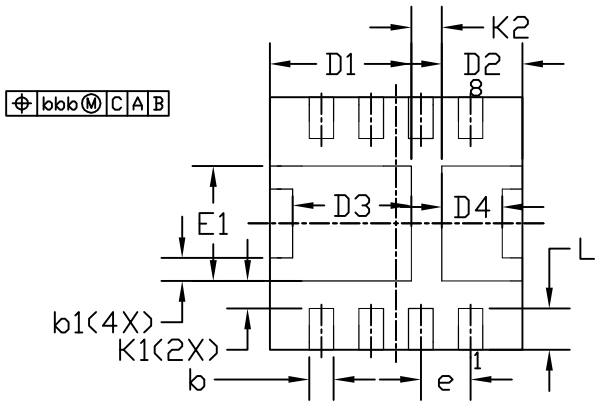
重庆万国

Document No.	POCQ-00011
Version	A

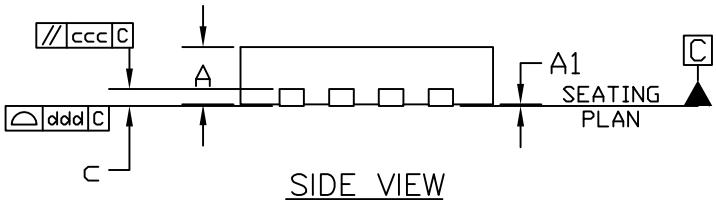
DFN3.3x3.3A_8L_EP2_S PACKAGE OUTLINE



TOP VIEW

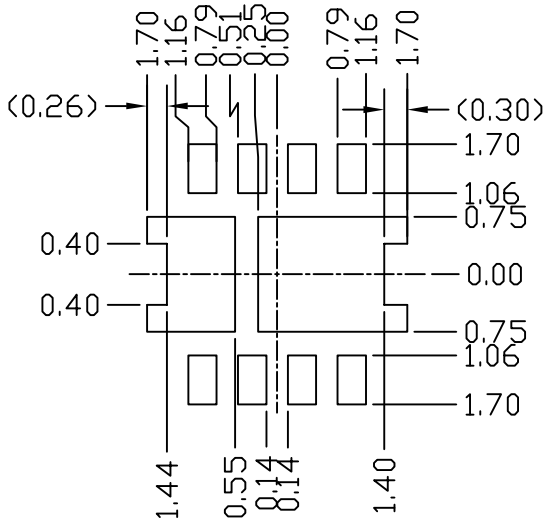


BOTTOM VIEW



SIDE VIEW

RECOMMENDED LAND PATTERN



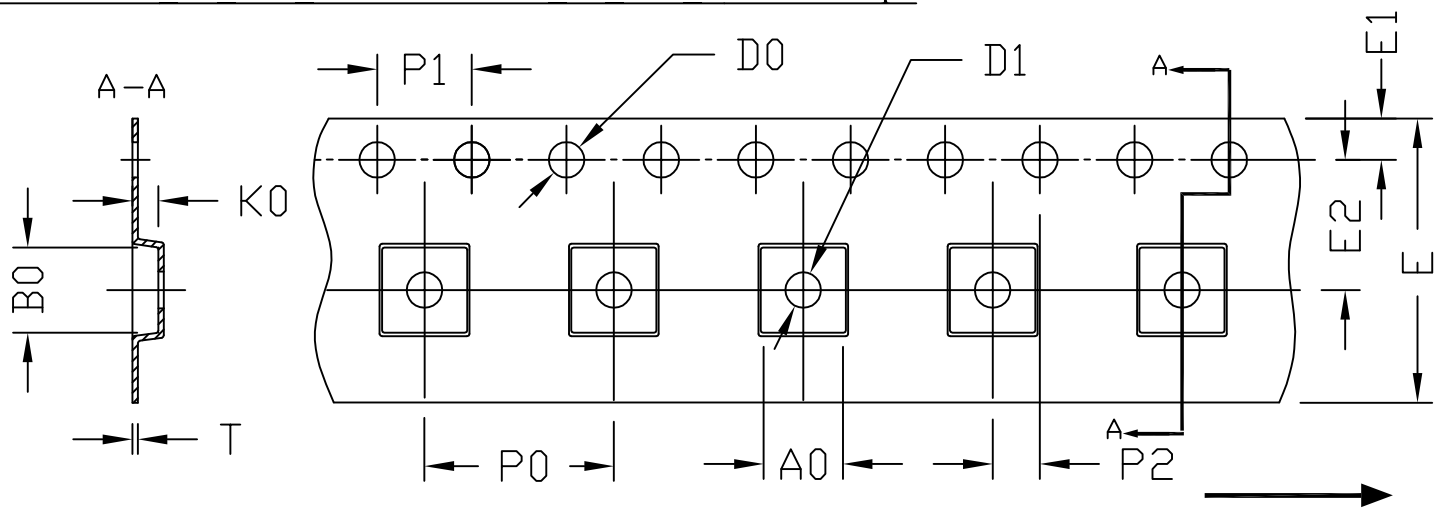
UNIT: mm

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.65	0.75	0.85	0.026	0.030	0.033
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.27	0.32	0.37	0.011	0.013	0.015
b1	0.25	0.30	0.35	0.010	0.012	0.014
c		0.203BSC			0.008BSC	
D	3.20	3.30	3.40	0.126	0.130	0.134
D1	1.75	1.85	1.95	0.069	0.073	0.077
D2	0.95	1.05	1.15	0.037	0.041	0.045
D3	1.45	1.55	1.65	0.057	0.061	0.065
D4	0.69	0.79	0.89	0.027	0.031	0.035
E	3.20	3.30	3.40	0.126	0.130	0.134
E1	1.40	1.50	1.60	0.055	0.059	0.063
e		0.65BSC			0.026BSC	
L	0.44	0.54	0.64	0.017	0.021	0.025
K1	0.26	0.36	0.46	0.010	0.014	0.018
K2	0.30	0.40	0.50	0.012	0.016	0.020
aaa		0.15			0.006	
bbb		0.10			0.004	
ccc		0.10			0.004	
ddd		0.08			0.003	

NOTE
1. CONTROLLING DIMENSION IS MILLIMETER.
   CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

DFN3.3x3.3_8L_EP1_S/DFN3.3x3.3A_8L_EP2_S Tape and Reel Data

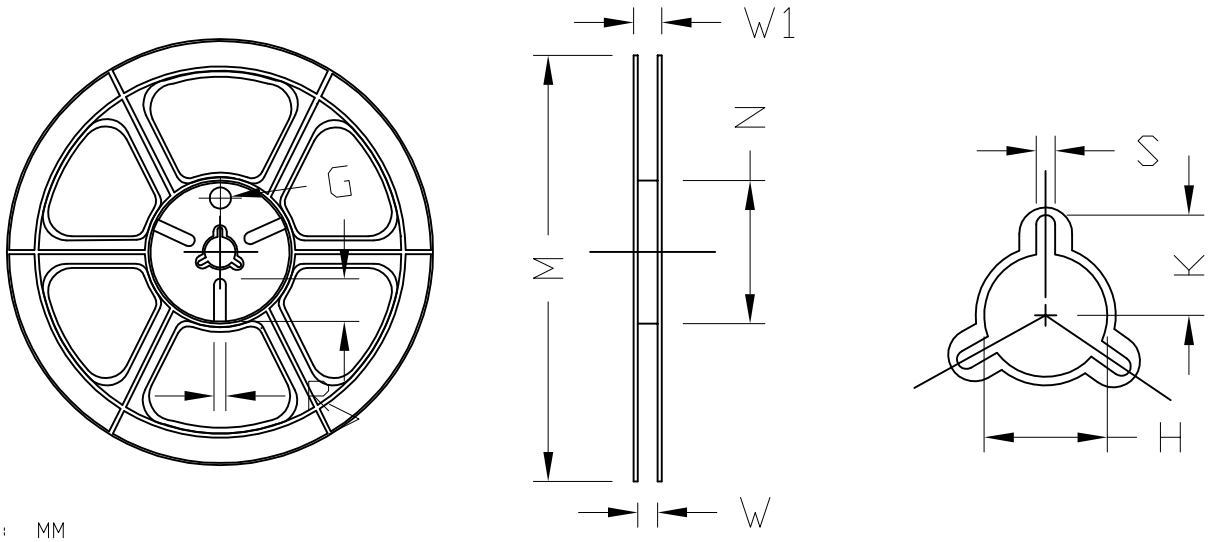
DFN3.3x3.3_8L_EP1_S/DFN3.3x3.3A_8L_EP2_S Carrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
DFN3.3x3.3	3.60 ±0.10	3.60 ±0.10	1.05 ±0.10	1.50 +0.10 −0	1.50 +0.10 −0	12.00 ±0.30	1.75 ±0.10	5.50 ±0.05	8.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.30 ±0.05

DFN3.3x3.3_8L_EP1_S/DFN3.3x3.3A_8L_EP2_S REEL



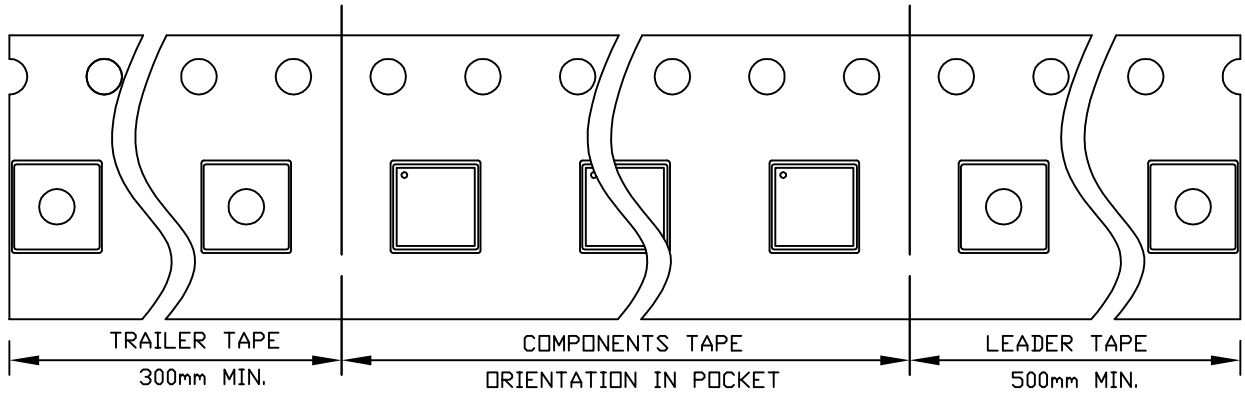
UNIT: MM

TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
12 mm	ø330	ø330.00 ±0.50	ø97.00 ±0.10	13.00 ±0.30	17.40 ±1.00	ø13.00 +0.50 −0.20	10.60	2.00 ±0.50	---	---	---

DFN3.3x3.3_8L_EP1_S/DFN3.3x3.3A_8L_EP2_S TAPE

Leader / Trailer & Orientation

Unit Per Reel: 3000pcs



CQAOS Semiconductor
Product Reliability Report

CQNE36132, rev A

Plastic Encapsulated Device

Chongqing Alpha & Omega Semiconductor, Limited

May, 2020

This CQAOS product reliability report summarizes the qualification result for CQNE36132. Accelerated environmental tests are performed on a specific sample size, and then followed by electrical test at end point. Review of final electrical test result confirms that CQNE36132 passes CQAOS quality and reliability requirements. The released product will be categorized by the process family and be routine monitored for continuously improving the product quality.

I. Reliability Stress Test Summary and Results

Test Item	Test Condition	Time Point	Total Sample Size	Number of Failures	Reference Standard
HTGB	Temp = 150°C , Vgs=100% of Vgsmax	168 / 500 / 1000 hours	462 pcs	0	JESD22-A108
HTRB	Temp = 150°C , Vds=100% of Vdsmax	168 / 500 / 1000 hours	462 pcs	0	JESD22-A108
Precondition (Note A)	168hr 85°C / 85%RH + 3 cycle reflow@260°C (MSL 1)	-	3927 pcs	0	JESD22-A113
HAST	130°C , 85%RH, 33.3 psia, Vds = 80% of Vdsmax	96 hours	693 pcs	0	JESD22-A110
Autoclave	121°C , 29.7psia, RH=100%	96 hours	924 pcs	0	JESD22-A102
Temperature Cycle	-65°C to 150°C , air to air,	1000 cycles	924 pcs	0	JESD22-A104
HTSL	Temp = 150°C	1000 hours	693 pcs	0	JESD22-A103
IOL	∆ Tj = 100°C	15000 cycles	693 pcs	0	MIL-STD-750 Method 1037

Note: The reliability data presents total of available generic data up to the published date.
Note A: MSL (Moisture Sensitivity Level) 1 based on J-STD-020

II. Reliability Evaluation

FIT rate (per billion): 3.82
MTTF = 29919 years

The presentation of FIT rate for the individual product reliability is restricted by the actual burn-in sample size. Failure Rate Determination is based on JEDEC Standard JESD 85. FIT means one failure per billion hours.

Failure Rate = $Chi^2 \times 10^9$ **/ [**2 (N) (H) (Af)**] =** 3.82
MTTF = 10^9 / FIT = 29919 years

Chi² = Chi Squared Distribution, determined by the number of failures and confidence interval
N = Total Number of units from burn-in tests
H = Duration of burn-in testing
Af = Acceleration Factor from Test to Use Conditions (Ea = 0.7eV and Tuse = 55°C)
Acceleration Factor [**Af**] = **Exp** [Ea / **k** (1/Tj u – 1/Tj s)]

Acceleration Factor ratio list:

	55 deg C	70 deg C	85 deg C	100 deg C	115 deg C	130 deg C	150 deg C
Af	259	87	32	13	5.64	2.59	1

Tj s = Stressed junction temperature in degree (Kelvin), K = C+273.16
Tj u =The use junction temperature in degree (Kelvin), K = C+273.16
k = Boltzmann's constant, 8.617164 X 10^{-5}eV / K